

proposed combination of U.S. Patent No. 6,208,545 to Leedy and European Patent Application No. EP1017100 to Shimoda et al. Applicants respectfully request reconsideration and withdrawal of these rejections because (1) one skilled in the art would not have been motivated to combine Leedy and Shimoda et al. and (2) the proposed combination does not teach each and every element recited in the claims.<sup>1</sup>

## **II. There Is No Motivation to Combine Leedy and Shimoda et al.**

In the Office Action, it was admitted that Leedy fails to teach a memory comprising a plurality of memory cells arranged in a plurality of layers stacked vertically above one another in a single chip, as recited in the claims. In an attempt to cure this deficiency, the Examiner proposed to replace the multi-chip structure disclosed in Leedy with the three-dimensional single chip/monolithic integrated circuit disclosed in Shimoda et al.<sup>2</sup> Applicants submit that one skilled in the art would not have been motivated to combine Leedy with Shimoda et al. because Leedy teaches away from the modification proposed in the Office Action.

Leedy repeatedly stresses the importance of using a multi-chip structure instead of a single chip, monolithic integrated circuit. In his background section, Leedy describes what he perceives to be disadvantages associated with single chips having high-density memories. Leedy explains that single chips having high-density memories require more sophisticated control circuitry, which requires an increased integrated circuit area. Increased integrated circuit area results in higher fabrication costs per integrated circuit (because there are fewer integrated circuits per wafer) and lower integrated circuit yields (because there are fewer working integrated

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<sup>1</sup> Applicants reserve the right to disqualify Shimoda et al. as prior art.

<sup>2</sup> In the Office Action, the Examiner noted that he has accepted the interpretation of "chip" as meaning "monolithic integrated circuit."

circuits per wafer). Leedy states that the objectives of his invention are to lower fabrication costs and increase performance by using a multi-chip structure *instead of a single chip*. Accordingly, Leedy teaches away from the very modification proposed in the Office Action – replacing a multi-chip structure with a single chip, monolithic integrated circuit. Because such a substitution would re-introduce the very problems that Leedy explicitly stated he wanted to avoid, one skilled in the art would not have been motivated to make the modification proposed in the Office Action. Accordingly, the 35 U.S.C. § 103(a) rejections of the claims based on the proposed combination of Leedy and Shimoda et al. must be withdrawn.

### **III. The Proposed Combination Does Not Teach Each of the Claim Elements**

Even assuming that one skilled in the art would have been motivated to combine Leedy and Shimoda et al., the 35 U.S.C. § 103(a) rejections must still be withdrawn because the proposed combination does not teach each and every element recited in the claims

#### **A. The Proposed Combination Fails to Teach a Modular Housing**

Independent Claims 114 and 117 require a modular housing that protects the error checking and correcting (ECC) code circuitry and the memory unit.<sup>3</sup> In the Office Action, it was asserted that this element is shown in Figures 1a and 1c in Leedy. Applicants respectfully disagree.

Figure 1a shows a memory device 100, a controller 101, a number of memory array circuit layers 103, and bond and interconnect layers 105. No where in Figure 1a is there a depiction of a housing protecting the memory array circuit layers 103 and error checking and

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<sup>3</sup> Claim 114: “a modular housing protecting the error checking and correcting (ECC) code circuitry and the memory unit”

Claim 117: “providing a modular, electronic memory device . . . comprising . . . a modular housing protecting the error checking and correcting (ECC) code circuitry and the memory unit”

correcting (ECC) code circuitry. To the contrary, all of the components in Figure 1a are shown as being exposed. Figure 1c also fails to show the recited housing. Figure 1c merely shows the memory device 100 of Figure 1a positioned face down on a larger integrated circuit or another three-dimensional memory device 107. As with Figure 1a, there is no showing of a housing protecting the memory unit and error checking and correcting (ECC) code circuitry.

**B. The Proposed Combination Fails to Teach a Modular Memory Device Adapted to be Releasably Connected to a Data Storage System**

Independent Claims 114, 117, and 120 require the recited memory device to be releasably connected to a data storage system.<sup>4</sup> As described in Applicants' specification, a user can readily connect the memory device to and later disconnect the memory device from a data storage system, such as a digital camera or a digital audio player. The ECC code circuitry carried by the memory device helps reduce or eliminate errors than can occur when the data storage system writes data to or reads data from the memory device.

Neither Leedy nor Shimoda et al. teaches a memory device releasably connectable to a data storage system, and, significantly, no attempt was made in the Office Action to assert that either reference contains such a teaching. At least some of the embodiments in Leedy describe the disclosed three-dimensional memory structure as being an embedded component in another circuit – not as a releasably connectable component to a data storage system, as recited in the claims. Shimoda et al. largely describes the manufacturing details of its memory structure and

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<sup>4</sup> Claim 114: "A modular three-dimensional electronic memory device adapted to be releasably connected to a data storage system"

Claim 117: "providing a modular, electronic memory device adapted to be releasably connected to a data storage system"

Claim 120: "a modular, electronic memory device adapted to be releasably coupled to the data storage system"

does not disclose any details regarding a data storage system that can be used with its memory structure, much less that its memory structure is releasably connectable to a data storage system.

**C. The Proposed Combination Fails to Teach a Data Storage System Comprising an ECC generator**

Independent Claim 120 recites a data storage system and a modular memory device adapted to be releasably coupled to the data storage system. Independent Claim 120 also recites that the data storage system comprises an error checking and correcting (ECC) code generator.<sup>5</sup> Accordingly, unlike independent Claims 114 and 117, which recite that ECC code circuitry *in the memory device* generates ECC bits, independent Claim 120 recites that ECC code circuitry *in the data storage system* generates ECC bits. This element is not shown in the proposed combination of Leedy and Shimoda et al. As a first matter, there is no discussion whatsoever in Shimoda et al. of ECC. Accordingly, for the rejection of Claim 120 to be proper, Leedy must disclose (1) a data storage system connectable to a memory device and (2) ECC code circuitry in the data storage system. Leedy does not teach either feature. As discussed above, there is no teaching in Leedy of a data storage system connectable to a memory device. While Leedy does disclose ECC logic, the ECC logic is part of the memory device controller, which also contains address decode and select logic and refresh and self-test logic. See Figure 2c and column 6, lines 52-66. The ECC logic is not part of a data storage system, as recited in independent Claim 120.

**IV. Conclusion**

The 35 U.S.C. § 103(a) rejections of Claims 114-124 based on the proposed combination of Leedy and Shimoda et al. should be withdrawn because (1) one skilled in the art would not have been motivated to combine Leedy and Shimoda et al. and (2) the proposed combination

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<sup>5</sup> Claim 120: “wherein the data storage system comprises an error checking and correcting (ECC) code generator”

does not teach each and every element recited in the claims. Reconsideration is respectfully requested.

If the Examiner has any questions concerning this Response, he is asked to contact the undersigned attorney at (312) 321-4719.

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Respectfully submitted,



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